CERTIFICATION OF TRANSLATION

I, ***Eun-Sook Lee***, an employee of Y.P.LEE, MOCK & PARTNERS of Koryo Bldg., 1575-1 Seocho-dong, Seocho-gu, Seoul, Republic of Korea, hereby declare under penalty of perjury that I understand the Korean language and the English language; that I am fully capable of translating from Korean to English and vice versa; and that, to the best of my knowledge and belief, the statement in the English language in the attached translation of ***Korean Patent Application No. 10-2002-0073049*** consisting of 18 pages have the same meanings as the statements in the Korean language in the original document, a copy of which I have examined.

Signed this 6th day of July 2006

Lee. E. S

ABSTRACT

[Abstract of the Disclosure]

Provided is a method for fabricating a semiconductor device. The method includes providing a semiconductor substrate in which a device formation region is defined, forming a gate including a gate dielectric layer and gate conductive layer and forming a sidewall spacer beside the sidewall of the gate for self-aligned contact formation at sidewalls on the device formation region, and forming a source region and a drain region at both sides of the gate of the semiconductor substrate, forming an etching stopper on the source region and the drain region, forming a first interlayer insulating film, which is planarized, on the whole surface of the semiconductor substrate, forming a self-aligned contact hole to expose the source region and the drain region by etching the first interlayer insulating film until it reaches the level of the upper layers of the sidewall spacer and the etching stopper by using dry etching, exposing the source region and the drain region by removing the etching stopper of the source region and the drain region by wet etching, and forming a contact pad by filling the self-aligned contact hole with dielectric polysilicon. As described above, if the self-aligned contact hole is formed by using wet etching, the silicon substrate of the source and drain regions is not damaged, and thus electric characteristics and reliability of the semiconductor device can be improved.

[Representative Drawing]

FIG. 8

SPECIFICATION

[Title of the Invention]

METHOD OF FABRICATING SEMICONDUCTOR DEVICE

[Brief Description of the Drawings]

FIGS. 1 and 2 are sectional views showing a method of fabricating a semiconductor device according to a conventional art;

FIGS. 3 through 7 are sectional views showing a method of fabricating a semiconductor device according to the present invention; and

FIG. 8 is a schematic flowchart showing a method of forming a self-aligned contact hole according to the present invention.

[Detailed Description of the Invention]

[Object of the Invention]

[Technical Field of the Invention and Related Art prior to the Invention]

The present invention relates to a method of fabricating a semiconductor device, and more particularly, to a method of forming a contact for a contact pad that connects with a source region and a drain region by using a self-aligned contact method.

As semiconductor devices become highly integrated, the distance between devices decreases, causing a limit to pattern formation process. In particular, when a contact is formed in an active region of a dynamic random access memory (DRAM) device, a contact area is smaller, which causes many problems in patterning. In order to solve these problems, a self-aligned contact formation has been introduced.

FIGS. 1 and 2 show a conventional self-aligned contact formation process. Referring to FIG. 1, an isolation insulating film 1110 is formed in a semiconductor substrate 100 to define a device formation region. A gate dielectric film 1121 (not shown) and gate conductive films 1123 and 1125 are formed in the device formation region, and an insulating film spacer 1129 is formed at the sidewalls of the gate

dielectric films 1123 and 1125 and a mask insulating film 1127 to form a gate 1120. A source region 1105a and a drain region 1105b are formed at both sides of the gate 1120. After an etching stopper 1140 is formed, a first interlayer insulating film 1150 is formed on the etching stopper 1140, and a self-aligned contact hole 1160a is formed in the first interlayer insulating film 1150 through a predetermined patterning process. Then, the etching stopper 1140 remaining in the self-aligned contact hole 1160a is removed by dry etching, and the source region 1105a and the drain region 1105b are exposed. After that, the contact hole 1160a is filled with conductive polysilicon to form a contact pad (not shown).

However, in the conventional self-aligned contact formation process, since the etching stopper 1140 remaining in the contact hole 1160a is etched by dry etching, a predetermined amount of over etching has to be performed to expose a silicon substrate. Thus the silicon substrate is damaged due to the characteristics of dry etching. Consequently, after a semiconductor device is manufactured, resistance of a contact hole 1160a that is damaged becomes high, causing contact failures and an increase in leakage current.

[Technical Goal of the Invention]

The present invention provides a method of fabricating a semiconductor device which has superior electric characteristics such as leakage current and contact resistance by not causing damage or stress to a silicon substrate when a self-aligned contact hole is formed in a source region and a drain region of the semiconductor device.

[Structure and Operation of the Invention]

According to one aspect of the present invention, there is provided a method for fabricating a semiconductor device including (a) providing a semiconductor substrate in which a device formation region is defined, (b) forming a gate including a gate dielectric layer and gate conductive layer and forming a sidewall spacer beside the sidewall of the gate for self-aligned contact formation at sidewalls on the device formation region, and

forming a source region and a drain region at both sides of the gate of the semiconductor substrate, (c) forming an etching stopper on the source region and the drain region, (d) forming a first interlayer insulating film, which is planarized, on the whole surface of the semiconductor substrate, (e) forming a self-aligned contact hole to expose the source region and the drain region by etching the first interlayer insulating film to the level of upper layers of the sidewall spacer and the etching stopper by using dry etching, (f) exposing the source region and the drain region by removing the etching stopper of the source region and the drain region by wet etching, and (g) forming a contact pad by filling the self-aligned contact hole with conductive polysilicon. Here, a gate insulating film is formed in a device formation region, and a gate dielectric film and a mask insulating film are sequentially formed in the gate insulating film. A gate pattern is formed in the gate dielectric film and the mask insulating film. An insulating film spacer is formed at sidewalls of the patterned gate dielectric film and the mask insulating film. The gate conductive films are formed of conductive polysilicon, and the mask insulating film is a silicon nitride film formed by chemical vapor deposition (CVD). The insulating film spacer is a silicon nitride film formed by CVD. Thus, the gate conductive films are surrounded by silicon nitride films, which prevents the gate conductive films from being damaged by the etchant solution used to etch silicon oxide films. The insulating film spacer and the mask insulating film are used as a mask when a contact hole is etched.

It is preferable that ion implantation be performed while a lower oxide film exists on the source and drain regions so as to prevent out diffusion of the implanted ions. Preferably, the gate dielectric film is used as the lower oxide film so as to simplify the whole process.

In order to form the etching stopper, a silicon nitride film is formed on the entire surface of the semiconductor substrate by using CVD. Here, the etching stopper may be a dual-layer by forming a buffer layer on the entire surface of the semiconductor device by using CVD prior to the formation of the etching stopper. The buffer layer is a silicon oxide film, and preferably, a mid-temperature oxide (MTO) film by using low pressure-chemical mechanical deposition (LP-CVD) so as to obtain a high etching

selectivity to other oxide films when the buffer layer is etched. The etching stopper is a silicon nitride film formed by using CVD.

In order to form the first interlayer insulating film, which is planarized, the first interlayer insulating film is formed on the entire surfaces of the semiconductor substrate and planarized by using a predetermined planarizing process. In particular, the first interlayer insulating film formed of silicon oxide by using high-density plasma chemical vapor deposition (HDP CVD) can have a high etching selectivity to the buffer film. Thus, a contact pattern can be kept firmly when the buffer film is wet etched. Preferably, the planarizing process is chemical mechanical process (CMP) which provides high flatness and does not produce a damage to the semiconductor substrate.

In order to form the self-aligned contact hole, a photoresist is formed which includes a self-aligned contact pattern on the planarized first interlayer insulating film. The first interlayer insulating film is removed by using the patterned photoresist as a mask and the self-aligned contact hole is formed. Here, the etching stopper, the mask insulating film, and the insulating film spacer are used as the etching stopper and function as masks.

The oxide film remaining on the etching stopper is removed by wet etching using an oxide etching solution or a nitride etching solution. Here, the oxide etching solution includes hydrofluoric acid (HF) having a density of 0.01 wt% through 0.001 wt%, and thus it is possible to remove polymers or residual particles occurring in dry etching, without causing any damage to the first interlayer insulating film. The nitride etching solution includes phosphoric acid H_3PO_4, the density of which is 50 wt% through 80 wt%.

If the buffer film is further formed between the etching stopper and the semiconductor substrate, the buffer film is removed to expose the source and drain regions. In the removal of the buffer film, an etching solution including ammonium hydroxide (NH_3OH), hydrogen peroxide (H_2O_2), and deionized water is used. Preferably, the wet etching is performed at a temperature of 30°C through 80°C. Here, the etching solution includes ammonium hydroxide (NH_3OH) having a density of 0.1 wt% through 1.0 wt% and hydrogen peroxide (H_2O_2) having a density of 4.0 wt%

through 7.0 wt%.

In order to form the contact pad, the self-aligned contact hole is filled by depositing the conductive polysilicon on the whole surface of the semiconductor substrate. The conductive polysilicon remains in the self-aligned contact hole by polishing the conductive polysilicon until it reaches the level of the upper portion of the first interlayer insulating film by using chemical mechanical polishing.

As described above, the etching stopper under the contact hole is removed by using wet etching when the contact hole is formed, so as not cause any damage to the source and the drain regions or any defect to a surface of the semiconductor substrate, and thus electric characteristics such as leakage current and contact resistance can be improved.

The present invention now will be described more fully with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete and will fully convey the concept of the invention to those skilled in the art.

FIGS. 3 through 7 are sectional views showing a method of fabricating a semiconductor device sequentially according to the present invention.

Referring to FIG. 3, an isolation insulating film 110 is formed in a semiconductor substrate 100 by using a predetermined isolation technology to define a device formation region. A gate dielectric film 121 is formed in the device formation region, and gate conductive films 123 and 125 and a mask insulating film 127 are sequentially formed. Here, the gate dielectric film 121 is either a silicon oxide film or a silicon nitride oxide film SiON. The gate conductive films 123 and 125 are formed by combining conductive polysilicon with metal silicide. In addition, the mask insulating film 127 is a silicon nitride film formed by chemical vapor deposition (CVD).

Photoresist (not shown) is formed in the mask insulating film 127, and a gate pattern is formed in the photoresist by using a predetermined alignment exposure process. The mask insulating film 127 is etched to form a hard mask 127 by dry

etching in which the patterned photoresist is used as a mask. After the photoresist used as a mask is removed, the gate pattern is transferred to the gate conductive films 123 and 125 by using the hard mask 127 as an etching mask. Then, a gate 120 is formed by forming an insulating film spacer 129 made of a silicn nitride film at the sidewalls of the hard mask 127 and the gate conductive films 123 and 125.

Hereinafter, the hard mask has the same reference numeral as the mask insulating film.

A source region 105a and a drain region 105b are formed on the semiconductor substrate 100 at both sides of the gate 120 by ion implantation in which the gate 120 is used as a mask. Here, a lower oxide film (not shown) may be formed in the source region 105a and the drain region 105b of the device formation region. The lower oxide film may be formed by thermal oxidation or may be the gate dielectric film 121 remaining in the device formation region.

A buffer layer 130 and the etching stopper 140 are sequentially formed on the whole surface of the semiconductor substrate 100. The buffer layer 130 serves as a stress buffering layer between the etching stopper 140 and the semiconductor substrate 100 in order to prevent stress from being applied to the semiconductor substrate 100 when the etching stopper 140 is formed. If the oxide film remains on the source region 105a and the drain region 105b, it may not be necessary to form the buffer layer 130. The buffer layer 130 is a silicon oxide layer formed by using chemical vapor deposition (CVD). In particular, it is desirable that the buffer layer 130 be a mid-temperature oxide film that is formed by using low pressure chemical vapor deposition and is deposited at a temperature of 500℃ through 600℃ because the buffer layer 130 can have a high etch rate and a high etching selectivity in an etch solution, i.e., ammonium hydroxide (NH4OH) solution. The etching stopper 140 is a silicon nitride film formed by using chemical vapor deposition (CVD) and has a high etching selectivity to the first interlayer insulating film 150 as the silicon oxide film. Thus, the etching stopper 140 is effective when the contact hole is formed.

After the first interlayer insulating film 150 is thickly formed on the whole surface of the semiconductor substrate 100, its surface is planarized by a predetermined

planarization process. If the hard mask 127a and the insulating film spacer 129 are nitride films in order to perform a self-aligned contact formation process, it is desirable that the first interlayer insulating film 150 be a silicon oxide film formed by using chemical vapor deposition (CVD) so that the first interlayer insulating film 150 can have a high etching selectivity with respect to the hard mask 127 and the insulating film spacer 129 as the silicon nitride films. In particular, it is desirable that the first interlayer insulating film 150 be a silicon oxide film formed by using high-density plasma chemical vapor deposition (HDP CVD) because the deposition is executed rapidly, and capability to fill the pattern is superior. When the etching stopper 140 and the buffer layer 130 are removed by wet etching, the first interlayer insulating film 150 formed by using HDP CVD is etched much slower than the etching stopper 140 and the buffer layer 130 by an etchant solution. Thus, damage (spoiling) to a contact pattern by wet etching can be reduced.

The first interlayer insulating film 150 can be planarized by using dry etching-back or chemical mechanical polishing (CMP). However, it is desirable that chemical mechanical polishing be used because it causes a small amount of damage to the semiconductor substrate 100.

After the planarization process is completed, it is desirable that the remaining thickness of the first interlayer insulating film 150 be higher than a predetermined height from an upper portion of the gate 120, thereby easily forming a self-aligned contact hole 160a of FIG. 6 when self-aligned contact hole etching is performed.

Referring to FIG. 4, the first interlayer insulating film 150 that is planarized is covered with a photoresist (not shown), and a self-aligned contact pattern is formed on the photoresist by using alignment exposure. Here, the self-aligned contact pattern is formed to connect the source region 105a with the drain region 105b. The self-aligned contact hole 160a is formed by etching the first interlayer insulating film 150 by dry etching in which the patterned photoresist is used as a mask. Here, an upper portion of the etching stopper 140 serves as an etching stopping boundary, and thus etching of the self-aligned contact hole 160a is stopped on the etching stopper 140. Then, the insulating film spacer 129 partially serves as a mask, and thus the self-aligned contact hole 160a is formed at sides of the insulating film spacer 129.

FIGS. 5 and 6 will be described with reference to a flowchart of FIG. 8.

Referring to FIGS. 5 through 8, the etching stopper 140 is removed by using wet etching to expose the buffer layer 130. An upper portion of the etching stopper 140 is cleaned by removing many residual products and polymers remaining on the semiconductor substrate 100 due to wet etching by using diluted hydrofluoric acid (HF) solution (step S1). Then, the silicon nitride film etching stopper 140 is removed by using an etching solution including phosphoric acid H_3PO_4 (step S2). Here, it is desirable that the etching solution including phosphoric acid H_3PO_4 be at a temperature of 120°C to 150°C to improve etching conditions, and have a density of 50wt% to 85wt% to obtain an appropriate etching rate. In general, the etching rate of the silicon oxide film (e.g., HDP silicon oxide film, HTO and MTO, or the like constituting the first interlayer insulating film 150) in the etching solution including phosphoric acid H_3PO_4 is 1Å through 4Å per minute.

Referring to FIGS. 6 through 8, the buffer layer 130 is removed by wet etching to expose the semiconductor substrate 100 of the source region 105a and the drain region 105b (step S3). Here, an etching solution is used to etch the silicon oxide film buffer layer and is an ammonium hydroxide (NH4OH) solution at a temperature of 30°C to 80°C. Thus, an etching rate of the silicon oxide film increases, and the time required by the entire process can be greatly reduced. While an etching process is in progress, the first interlayer insulating film 150, which is a silicon oxide film formed by using HDP CVD, is also etched. However, an etching rate of the first interlayer insulating film 150 is about 2Å per minute. Since the etching speed of the first interlayer insulating film 150 is slower than that of the buffer layer 130 as the etching rates of a mid-temperature oxide (MTO) film, the buffer layers 130, and the first interlayer insulating film 150 are about 5Å and hundreds of Å respectively while thousands of Å of the first interlayer insulating film 150 is etched per minute. Therefore, this wet etching hardly causes damage the contact hole morphology considering changes in sizes of the contact hole.

The etching solution should have a high etching rate with respect to the buffer layer 130 and a low etching rate to the first interlayer insulating film 150. Thus, the etching solution is formed by combining ammonium hydroxide (NH_4OH), hydrogen

peroxide (H_2O_2), and deionized water. In particular, the etching solution of the oxide film should include 0.1 wt% through 1.0 wt% of ammonium hydroxide, and 4.0 wt% through 7.0 wt% of hydrogen peroxide. Thus, when the buffer layer 130 is etched, the first interlayer insulating film 150 can keep the self-aligned contact hole 160a pattern firmly. The etching solution including ammonium hydroxide (NH_4OH) does not causes damage to the silicon substrate of the semiconductor substrate 100, and thus the source region 105a and the drain region 105b can be exposed without causing any defects or stress.

Referring to FIG. 7, enough conductive polysilicon is formed on the whole surface of the semiconductor substrate 100 to fully fill the self-aligned contact hole 160a. Then, the conductive polysilicon is removed by chemical mechanical polishing it until it reaches the level of the upper portion of the first interlayer insulating film 150. Then, the self-aligned contact hole 160a is filled with the conductive polysilicon, and thus a contact fill or a contact pad 160 is formed.

As described above, the method for fabricating a semiconductor device according to the present invention removes the etching stopper 140 and the buffer layer 130 by using wet etching when the contact hole is formed, and thus an additional cleaning process is not needed.

That is, when the contact hole is formed according to the conventional method, the etching stopper 140 is removed by using wet etching to expose the semiconductor substrate 100, and then is further cleaned to remove polymers or residual particles due to wet etching. Thus, the time required for forming the contact hole increases.

However, in the present invention, the etching stopper 140 and the buffer layer 130 are etched by using wet etching. In particular, the ammonium hydroxide (NH_4OH) solution, which is used to etch the buffer layer 130, also serves as a cleaning solution, and thus an additional cleaning process is not needed. As a result, the time required for forming the contact hole is reduced to a half of the time required for the conventional method.

While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that

various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

[Effect of the Invention]

According to the present invention, the etching stopper under the contact hole is removed by using wet etching when the contact pad connecting the source region with the drain region is formed, not causing any damage to the source and the drain regions or any defect to a surface of the semiconductor substrate. Thus electrical characteristics such as leakage current and contact resistance can be improved.

What is claimed is:

1. A method for fabricating a semiconductor device, the method comprising:

(a) providing a semiconductor substrate in which a device formation region is defined;

(b) forming a gate including a gate dielectric layer and gate conductive layer and forming a sidewall spacer beside the sidewall of the gate for self-aligned contact formation at sidewalls on the device formation region, and forming a source region and a drain region at both sides of the gate of the semiconductor substrate;

(c) forming an etching stopper on the source region and the drain region;

(d) forming a first interlayer insulating film, which is planarized, on the whole surface of the semiconductor substrate;

(e) forming a self-aligned contact hole to expose the source region and the drain region by etching the first interlayer insulating film to the level of upper layers of the sidewall spacer and the etching stopper by using dry etching;

(f) exposing the source region and the drain region by removing the etching stopper of the source region and the drain region by wet etching; and

(g) forming a contact pad by filling the self-aligned contact hole with conductive polysilicon.

2. The method of claim 1, wherein, in step (b), the gate further includes a hard mask on the surface of the gate conductive layer.

3. The method of claim 1, wherein the sidewall spacer for self-aligned contact formation and the etching stopper are silicon nitride films formed by using chemical vapor deposition, and the first interlayer insulating film is a silicon oxide film formed by using chemical vapor deposition (CVD).

4. The method of claim 3, wherein the first interlayer insulating film is a silicon oxide film formed by using high-density plasma chemical vapor deposition (HDP CVD).

5. The method of one of claims 1, 3, and 4, wherein the method further comprises forming a buffer layer on the source region and the drain region prior to step (c) and removing the buffer layer by using wet etching after step (f).

6. The method of claim 5, wherein the buffer layer is a silicon oxide film formed by using thermal oxidation.

7. The method of claim 6, wherein the buffer layer is a mid-temperature oxide (MTO) film formed by using low pressure chemical vapor deposition (LP CVD).

8. The method of claim 1, wherein the etching stopper is a silicon nitride film formed by using chemical vapor deposition.

9. The method of claim 3, wherein the first interlayer insulating film is a silicon oxide film formed by using high-density plasma chemical vapor deposition.

10. The method of claim 1, wherein step (f) further comprises:

removing remaining oxide film on the etching stopper by using wet etching by using an oxide etchant; and

removing the etching stopper by using an etching solution or oxide etching solution nitride.

11. The method of claim 10, wherein the oxide etching solution includes hydrofluoric acid (HF) having a density of 0.01 wt% through 0.001 wt%.

12. The method of claim 10, wherein the nitride etching solution includes phosphoric acid H_3PO_4.

13. The method of claim 12, wherein the density of phosphoric acid H_3PO_4 is 50 wt% through 80 wt%.

14. The method of claim 5, wherein the buffer layer is removed by using an etching solution including ammonium hydroxide (NH_3OH), hydrogen peroxide (H_2O_2), and deionized water.

15. The method of claim 14, wherein the etching solution includes ammonium hydroxide (NH_3OH) having a density of 0.1 wt% through 1.0 wt%.

16. The method of claim 14, wherein the etching solution includes hydrogen peroxide (H_2O_2) having a density of 4.0 wt% through 7.0 wt%.

17. The method of claim 14, wherein the wet etching is performed at a temperature of 30℃ through 80℃.

18. The method of claim 1, wherein step (g) further comprises:

filling the self-aligned contact hole by depositing the conductive polysilicon on the whole surface of the semiconductor substrate; and

remaining the conductive polysilicon in the self-aligned contact hole by polishing the conductive polysilicon until it reaches the level of the upper portion of the first interlayer insulating film by using chemical mechanical polishing.

FIG. 1 (PRIOR ART)

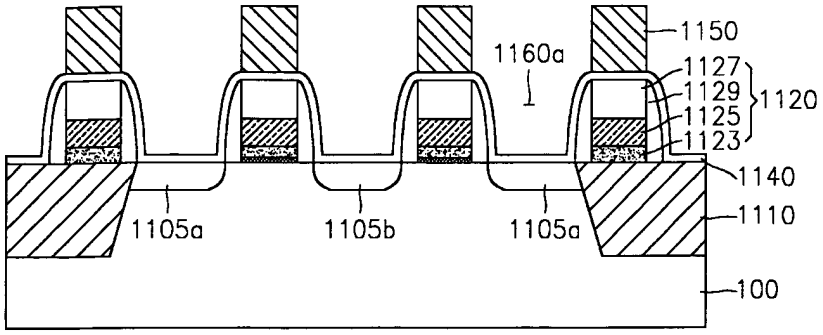

FIG. 2 (PRIOR ART)

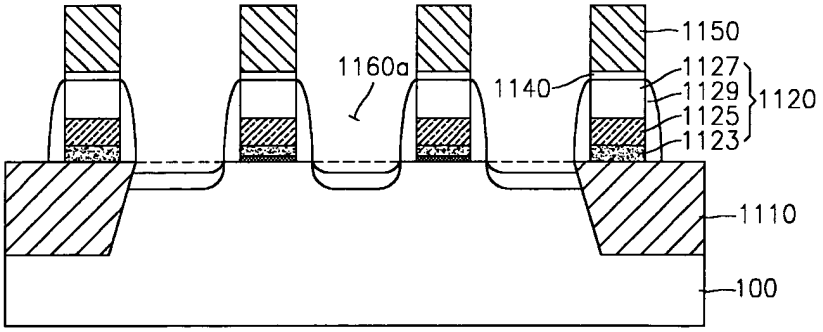

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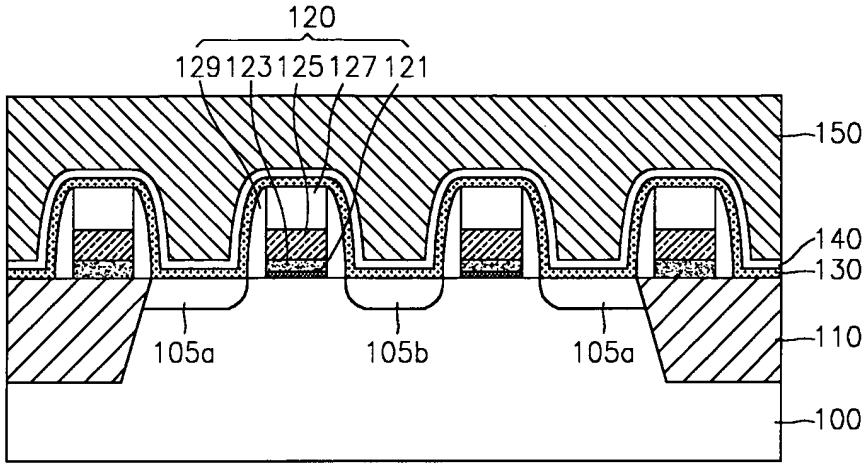
FIG. 3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105a
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FIG. 4

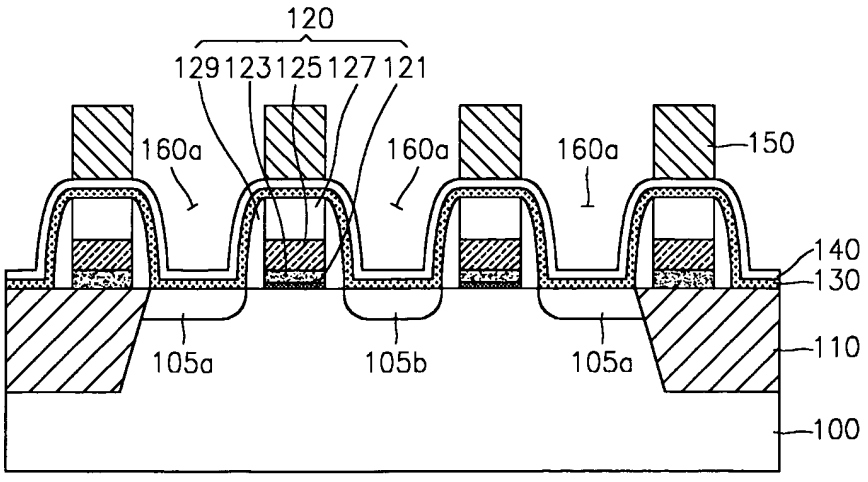
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FIG. 5

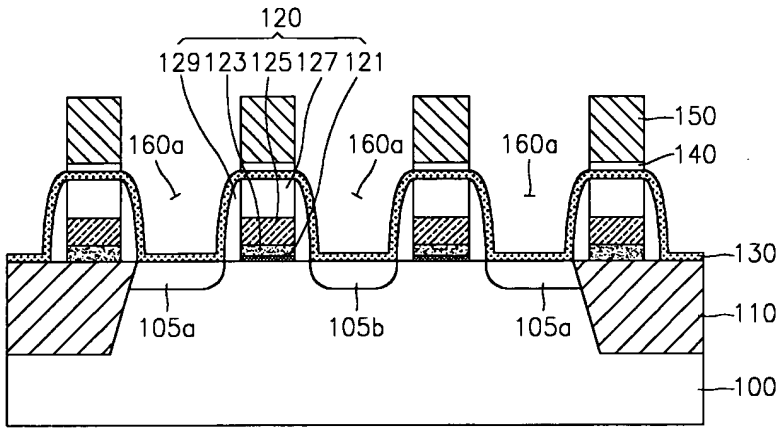
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FIG. 6

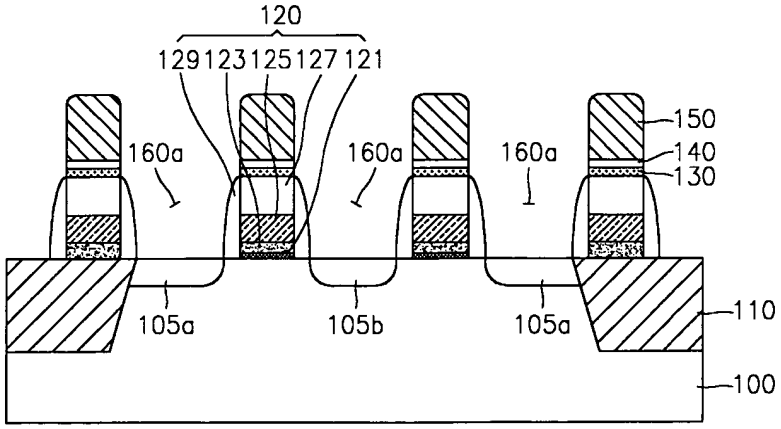
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FIG. 7

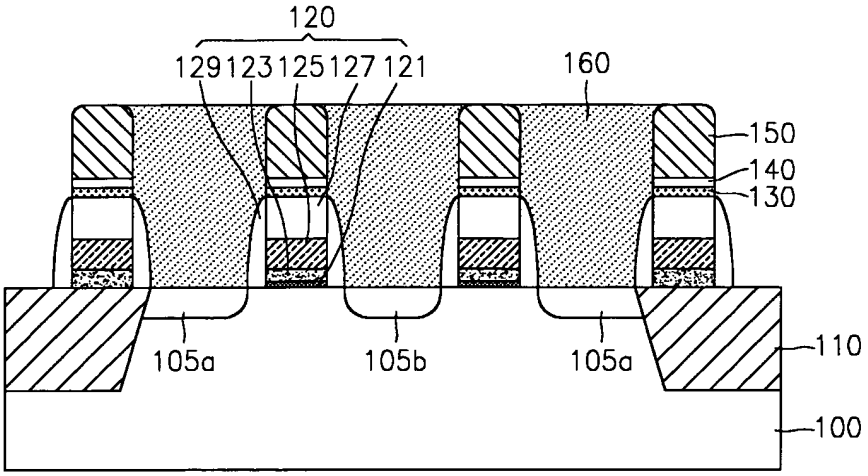
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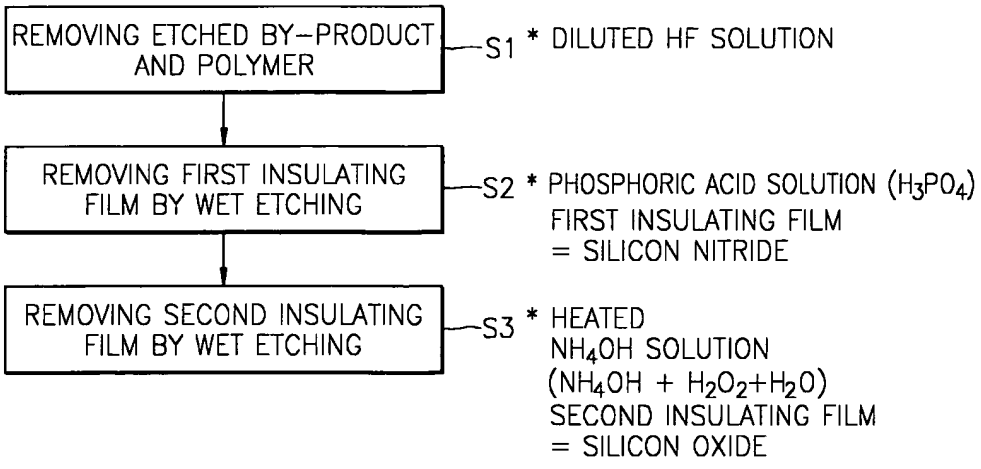
FIG. 8


REMOVING ETCHED BY-PRODUCT AND POLYMER
S1
* DILUTED HF SOLUTION
REMOVING FIRST INSULATING FILM BY WET ETCHING
S2
* PHOSPHORIC ACID SOLUTION (H_3PO_4)
FIRST INSULATING FILM = SILICON NITRIDE
REMOVING SECOND INSULATING FILM BY WET ETCHING
S3
* HEATED NH_4OH SOLUTION ($NH_4OH + H_2O_2 + H_2O$)
SECOND INSULATING FILM = SILICON OXIDE